Voltafield

Three-Axis Geomagnetic Sensor IC

VTC AF8133J
Data Sheet

Version 0.3(Preliminary)- May/31/2016

Table of Contents

Revision History

Rev.	Date	Chapter	Contents of Changes	Originator
0.1	Feb/26/2016		Initial release.	Grant Cheng
0.2	May/19/2016	Chap. 2.3 Chap. 2.4	Marking Information updated AVDD = DVDD = 1.68V~3.6V…	Kyan Chao
0.3	May/31/2016	Chap. 2.2 Chap. 3.1 Chap. 5.1	… to Ground or DVDD or AVDD. AVDD, DVDD related Pin A0 connected…	Kyan Chao

1. Product Features and Applications

1.1 General Description

VTC's AF8133J is a 3-axis magnetic sensor designed for geomagnetic field sensing applications such as e-Compass and motion sensing. The AF8133J utilizes VTC's proprietary Anisotropic Magneto Resistive (AMR) technology which provides advantages over the conventional Hall Effect sensors. The advantages include lower noise density, better magnetic field interference immunity. The AF8133J's internal 16-bit ADC provides high resolution outputs for users to access through its I^2C digital serial interface. AF8133J is in Wafer Level Chip Scale Package (WLCSP). It is pin to pin compatible with VTC's AF8133I.

1.2 Product Features

- 3-axis magneto resistive sensors and ASIC in 1.2*1.2*0.5 mm WLCSP.
- Magnetic field range is ± 2200 μT typically.
- High resolution 0.036 μT/LSB @ ±1200 μT with 16-bit ADC.
- Low noise density.
- Support single power source.
- 400Hz Maximum output rate.
- Low power consumption (145 μA @ 10Hz).
- I^2C interface.
- Lead free package construction.

1.3 Applications

- E-Compass
- Navigation
- Indoor Navigation
- Magnetometer
- Robots
- Consumer electronics
- Wearable devices

2. Circuit Diagram and Pin Assignments

2.1 Circuit Diagram

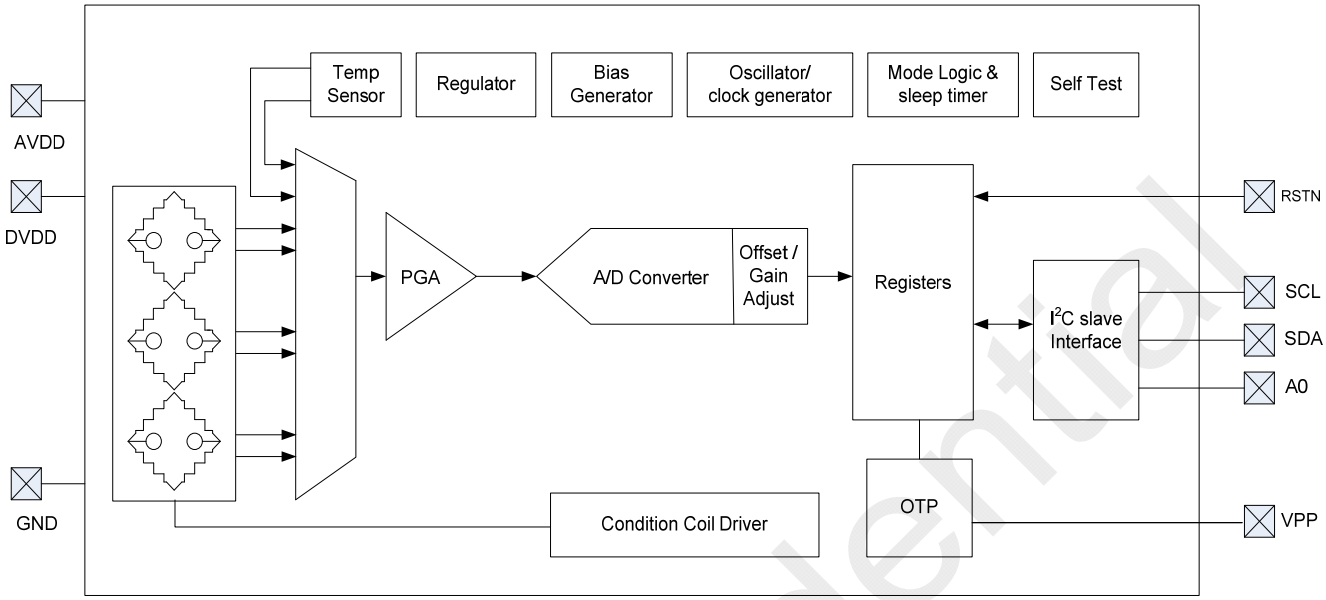


Fig. 1 *Block Diagram*

Table 1. *AF8133J Block description*

Block Name	Description
Temp Sensor	Temperature compensation for magnetic sensors.
Regulator	Provide power supply for magnetic sensors and digital block.
Bias Generator	Generate bias current for sensors and circuits.
Oscillator/clock generator	Provide internal clock.
Mode Logic & sleep timer	Change state to measurement or sleep by user command.
PGA	Pre-amplifier used to amplify the magnetic sensor signal.
A/D Converter	Perform analog-to-digital conversion with 16-bits resolution.
Offset / Gain Adjust	Offset and gain adjustment for the system.
Registers	Store measurement data and user configuration.
I^2C slave Interface	Exchange data with external CPU.
Condition Coil Driver	Magnetic sensor driver circuit for sensor initialization.

2.2 Pin Description

Table 2. *Pin Descriptions*

Pad No.	Pin Name	Function
A1	AVDD	Analog power supply.
A2	A0	I^2C address selection. Connect to Ground or DVDD or AVDD.
A3	VPP	Factory usage only. Connect to Ground.
B1	GND	Supply Ground.
B3	SCL	I^2C serial clock input.
C1	DVDD	Digital power supply.
C2	RSTN	Reset pin. Active low.
C3	SDA	I^2C serial data input / output.

2.3 Pin Assignment and Relationship between the Magnetic Field and Output Code

[AF8133J]

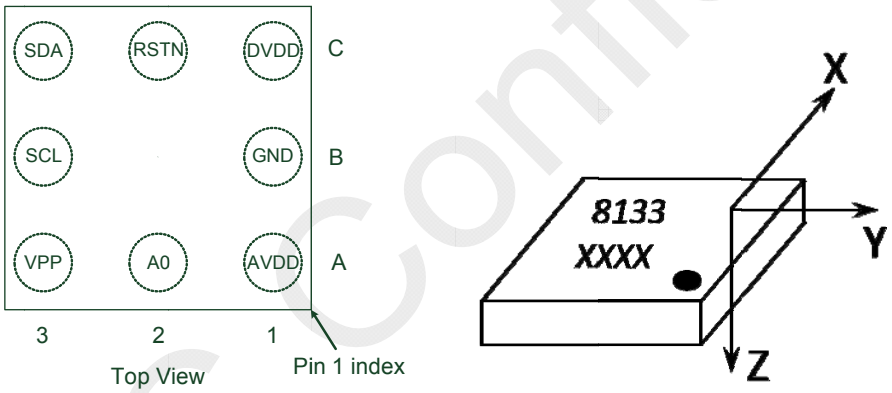


Fig. 2 *Pin Assignment & the Definition of Orientation*

Marking Information:

Product Name : 8133
Trace Code : $X_1X_2X_3X_4$

X_1= R or A, production information
$X_2X_3X_4$ = Date Code

2.4 Recommended External Connection

< AF8133J>

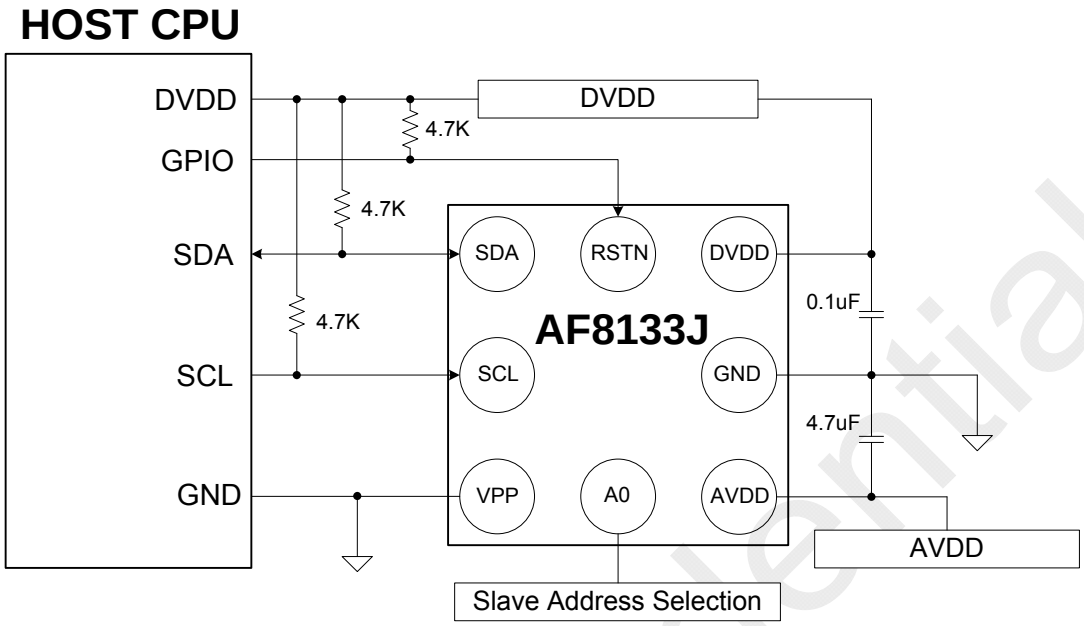


Fig. 3 *Dual Power Reference Design*

Note: AVDD = DVDD = 1.68V~3.6V is a compatible design.

2.5 Dimensions Outline

[AF8133J]

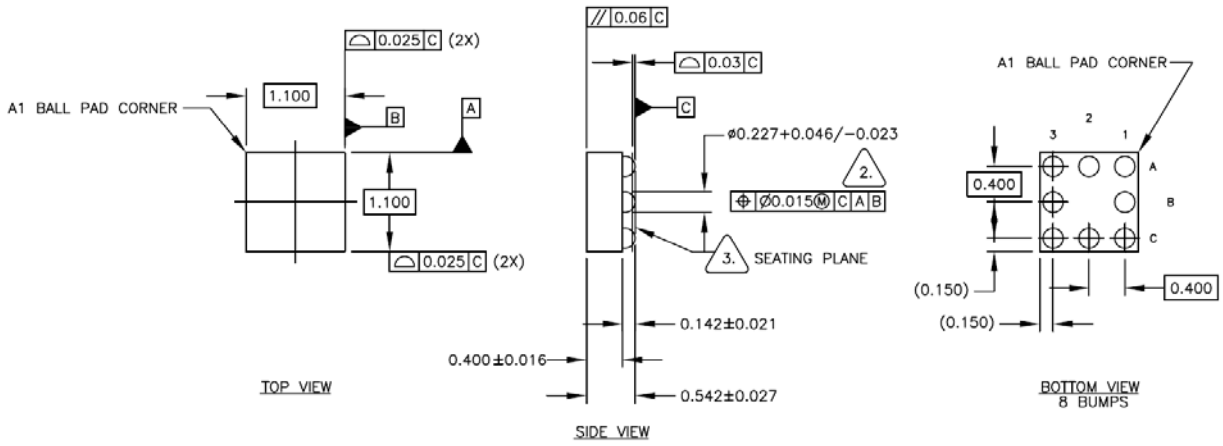


Fig. 4 *Dimensions Outline*

3. Specifications

3.1 Specifications

(Measurements @ 25℃, unless otherwise noted; AVDD=2.8V, DVDD=1.8V unless otherwise specified)

Table 3. *SPEC Table*

Characteristics	Conditions	Min	Typ	Max	Unit
Power Supply					
Supply Voltage	AVDD referenced to GND	1.68	2.8	3.6	V
	DVDD referenced to GND	1.68	1.8	AVDD	V
Standby State Current	DVDD + AVDD	-	0.6	3	μA
Operation supply current*1	Output data rate @ 10Hz	-	170	-	μA
	Output data rate @ 100Hz	-	1700	-	μA
	Output data rate @ 10Hz ; **AVDD=DVDD=1.8V**	-	145*2	-	μA
	Output data rate @ 100Hz ; **AVDD=DVDD=1.8V**	-	1450*2	-	μA
Performance					
Field Range*	Full scale (FS) – total applied field (Typical)	-2200		+2200	μT
Resolution	16-bit ADC@ ±1200 μT	-	0.036	-	μT/LSB
Linearity	Best Fit Linear Curve @ ± 300 μT (XY/Z axis)	-	0.2/0.4	-	%FS
Hysteresis	3 sweeps across ±300 μT	-	1.8	-	%FS
General					
Operating Temperature	Ambient	-30		85	°C

1Note : Operation by VTC proprietary algorithm.

2Note : It is a design reference that the operation supply current is at AVDD=DVDD=1.8V.

Note: Field strength > ±1800 uT sweep might encounter higher Hysteresis in Z axis

3.2 Absolute Maximum Ratings

Table 4. *Absolute Maximum Ratings*

Symbol	Parameter	Min	Max	Unit
AVDD	Supply voltage	-0.3	4.0	V
DVDD	I/O pin supply voltage	-0.3	AVDD	V
ESD Voltage	Human body mode Machine mode		3000 200	V
Storage Temperature	Ambient, unbiased	-40	95	°C

Note: Stress above these limits may cause damage to the devices.

3.3 I²C and I/O Characteristics

Table 5. *I²C and I/O Electrical Characteristics*

Parameter	Symbol	MIN	MAX	Unit
LOW level input voltage	V_{IL}	-0.3	0.35*DVDD	V
HIGH level input voltage	V_{IH}	0.6*DVDD	-	V
Hysteresis of Schmitt trigger inputs	V_{hys}	0.05*DVDD	-	V
Output voltage, pin SDA (open drain), $I_{OL} \leqq 1$ mA	V_{OL}	-	0.25	V
Input current, pins SDA and SCL (input voltage between 0.1*DVDD and 0.9*DVDD max)	I_{IH}	-10	10	μA

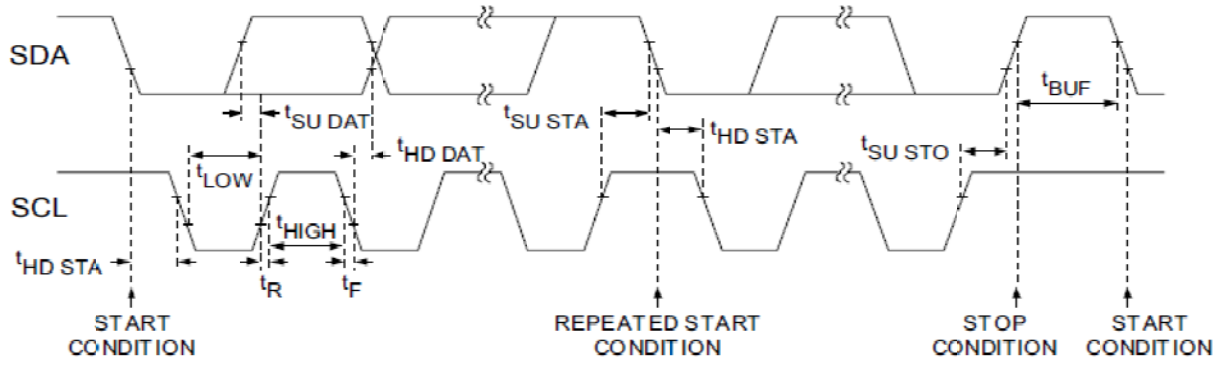
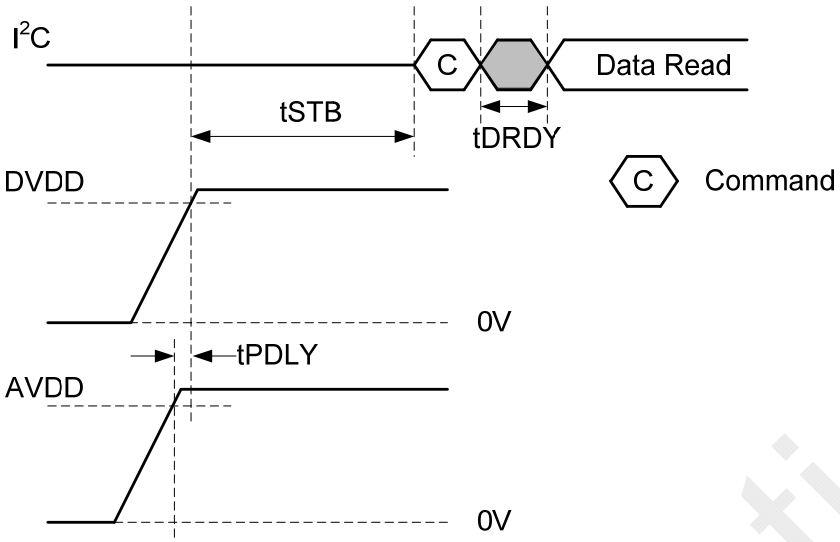


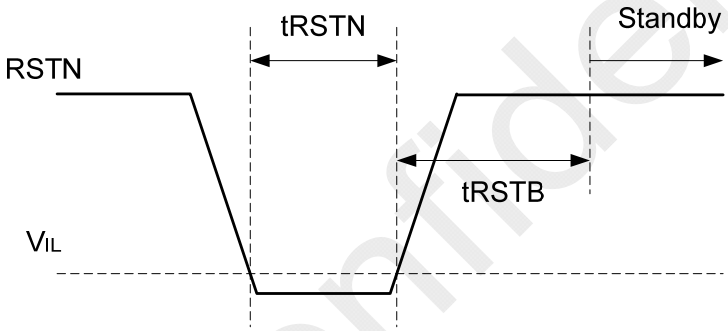
Fig. 5 I²C Interface Timing

Table 6. *I²C Timing Characteristics*

Parameter	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency.	0	100	0	400	kHz
$t_{HD;\ STA}$	Hold time (repeated) START condition.	4	-	0.6	-	μs
t_{LOW}	LOW period of the SCL clock.	4.7	-	1.3	-	μs
t_{HIGH}	HIGH period of the SCL clock.	4	-	0.6	-	μs
$t_{SU;STA}$	Set-up time for a repeated STAR condition.	4.7	-	0.6	-	μs
$t_{HD;DAT}$	Data hold time.	5	-	-	-	μs
$t_{SU;DAT}$	Data set-up time.	250	-	100	-	ns
$t_{SU;STO}$	Set-up time for STOP condition.	4	-	0.6	-	μs
t_{BUF}	Bus free time between a STOP and START.	4.7	-	1.3	-	μs

Note: Values are based on I²C Specification requirements, not tested in production.





Parameter	Condition	Min	Max	Units
tPDLY	Power delay time.	0		µs
tSTB	Period of time from power on to standby.	15		ms
tDRDY	Period of time from standby to data ready.	1		ms
tRSTB	Period of time from reset to standby.	1		ms
tRSTN	Reset pin active pulse width.	5		µs

4. Operation

4.1 Operational States

The AF8133J has two states after power on/reset and initialization. The main purpose is for power saving and data synchronization. A simplified state diagram is shown below.

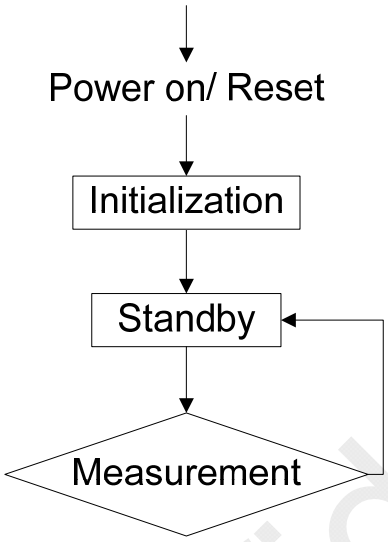


Fig. 6 *State Diagram*

4.1.1 Initialization

Register setting for application and calibration.

4.1.2 Standby

The Standby state offers the lowest power consumption. In this state, the I^2C interface is active and all register reads and writes are allowed. There is no measurement in the Standby state and the internal clocking is halted. Complete access to the register set is allowed in this state. AF8133J defaults to the Standby state after power-on or software-reset.

4.1.3 Measurement

Magnetic sensor measurement is started. After measurement and data process finished, measurement data is stored to registers (0x03 to 0x08), and then AF8133J transits to the standby state with the state register changed to reflect the standby state.

4.2 Measurement Configuration

4.2.1 Magnetic Field Range

The magnetic field range is programmable in ranges from ±1200 μT to ± 2200 μT. The programmable option is designed to meet the requirements for different applications because the field range and sensitivity are inversely correlated. For instance, the device can be set to the lowest possible field range to gain the highest sensitivity. See also Section 6.5 Field Range Register (0x0B).

4.2.2 Measurement & Data Read Timing

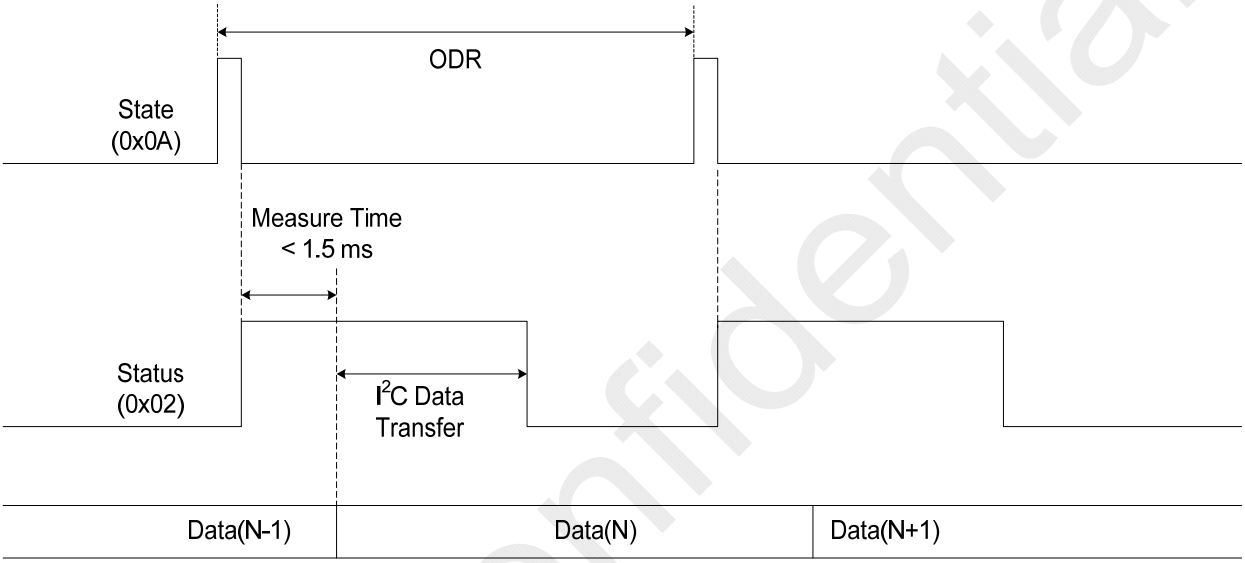


Fig. 7 *Measurement Timing*

5. I²C Interfaces

AF8133J always operates as an I²C slave on I²C interfaces. The I²C slave interface works at a maximum speed of 400 kHz, also for 100kHZ, standard mode. The SDA (data) are open-drain, bi-directional pins and the SCL (clock) are input pins. Both SCL and SDA require an external pull-up resistor, typically 4.7kΩ. An I²C master device initiates all communication and data transfers and generates the SCL clock that synchronizes the data transfer. AF8133J's I²C device address is 0x1E or 0x1C, which is depending on pin A0's connection. (Refer to section 5.1 for more detail). The I²C interface remains active as long as power is applied to the DVDD pin. AF8133J data can be Read/Write continuously with non-stop bit between I²C transactions.

5.1 Slave Addresses

The Slave address is configurable through the use of pin A0. The table below shows this relationship. Pin A0 connected to GND that is for the default configuration.

Table 7. *Slave Base Address Options*

Pin A0	7-Bit I²C Address		8-Bit Address	
			Write	Read
GND	0b0011110	0x1E	0x3C	0x3D
DVDD or AVDD	0b0011100	0x1C	0x38	0x39

5.2 Timing

See Section 3.3 I²C Timing Characteristics for I²C timing requirements.

5.3 I²C Message Format

AF8133J uses the following general format for writing to the internal register (Take 0x1E for example). The I²C master generates a START condition, and then follows the device ID. The 8th bit is the R/W flag (write cycle = 0). AF8133J pulls SDA low during the 9th clock cycle indicating a positive ACK.

The second byte is the 8-bit register address of the device to access, and the last byte is the data to write.

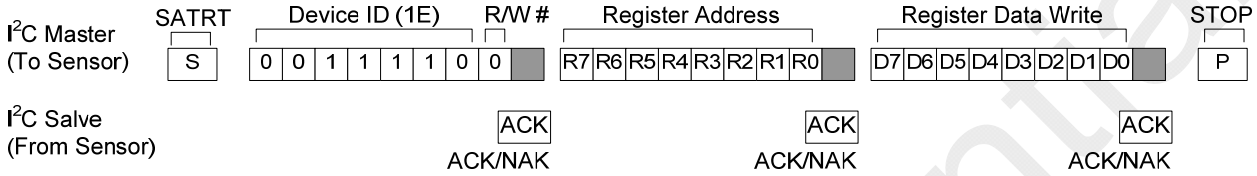


Fig. 8 *I²C Message Format, Write Cycle, Single Register Write*

In a read cycle, the I²C master device writes the device ID (R/W =0) and the register address to be accessed. The master device issues a RESTART condition and then writes the device ID with the R/W flag set to '1'. The device shifts out the contents of the register address.

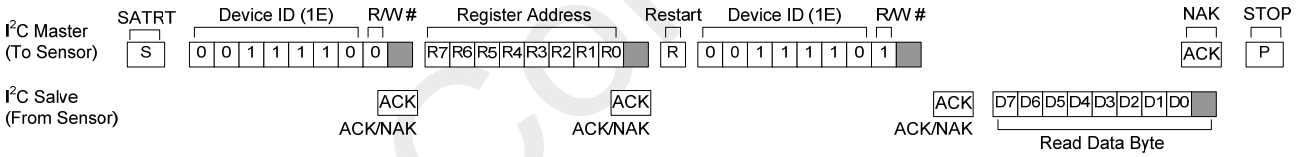


Fig. 9 *I²C Message Format, Read Cycle, Single Register Read*

The I²C master device may write or read consecutive register addresses by writing or reading additional bytes after the first access. AF8133J will internally increment the register address.

6. Register Interface

AF8133J has a simple register interface which allows a MCU or I^2C master to configure and monitor all aspects of the device. This section lists an overview of AF8133J's user programmable registers.

Table 8. *Register Summary*

Addr (Hex)	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
00	PCODE	PCODE[7]	PCODE[6]	PCODE[5]	PCODE[4]	PCODE[3]	PCODE[2]	PCODE[1]	PCODE[0]	0x5E	R
02	STATUS	0	0	0	0	0	0	0	ACQ	0x00	R
03	CH1_LSB	CH1[7]	CH1[6]	CH1[5]	CH1[4]	CH1[3]	CH1[2]	CH1[1]	CH1[0]	0x00	R
04	CH1_MSB	CH1[15]	CH1[14]	CH1[13]	CH1[12]	CH1[11]	CH1[10]	CH1[9]	CH1[8]	0x00	R
05	CH2_LSB	CH2[7]	CH2[6]	CH2[5]	CH2[4]	CH2[3]	CH2[2]	CH2[1]	CH2[0]	0x00	R
06	CH2_MSB	CH2[15]	CH2[14]	CH2[13]	CH2[12]	CH2[11]	CH2[10]	CH2[9]	CH2[8]	0x00	R
07	CH3_LSB	CH3[7]	CH3[6]	CH3[5]	CH3[4]	CH3[3]	CH3[2]	CH3[1]	CH3[0]	0x00	R
08	CH3_MSB	CH3[15]	CH3[14]	CH3[13]	CH3[12]	CH3[11]	CH3[10]	CH3[9]	CH3[8]	0x00	R
0A	STATE	0	0	0	0	0	STATE[2]	STATE[1]	STATE[0]	0x00	R/W
0B	RANGE	RNGE_21 [3]	RNGE_21 [2]	RNGE_21 [1]	RNGE_21 [0]	RNGE_3 [3]	RNGE_3 [2]	RNGE_3 [1]	RNGE_3 [0]	0x34	R/W
11	SWR	SWR	0	0	0	0	0	0	SWR	0x00	R/W

6.1 [0x00] Product Code

These registers represent product code of AF8133J.

Table 9. *Product Code Register*

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
00	PCODE	PCODE [7]	PCODE [6]	PCODE [5]	PCODE [4]	PCODE [3]	PCODE [2]	PCODE [1]	PCODE [0]	0x5E	R

6.2 [0x02] Status Register - Behavioral Flags

Table 10. *Status Register*

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
02	STATUS	0	0	0	0	0	0	0	ACQ	0x00	R

Table 11. *Status Register Bits*

ACQ	**Acquisition Bit** This bit indicates new data is available in the Output registers or has been read. 0: Output data has been read. 1: Unread Output data is available. This bit is cleared when one or more of the output registers have been read.

6.3 [0x03-0x08] Output Registers

Upon completion of a measurement, data is placed in the registers shown below. If the data in the output register has not been read when new data is ready, the unread data in the output register is being replaced by the new data. All three channels are updated simultaneously. To prevent an erroneous situation where data is being read at the same time when new data is ready, a lock condition has been implemented. New data will not be placed in this output register until an I^2C Stop bit has been issued.

The output registers contain 16-bit, 2's complement values. Per standard notation, bit [15] is the MSB and bit [0] is the LSB.

Table 12. *Output Register Table*

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x03	Ch1_LSB	CH1[7]	CH1[6]	CH1[5]	CH1[4]	CH1[3]	CH1[2]	CH1[1]	CH1[0]	0x00	R
0x04	Ch1_MSB	CH1[15]	CH1[14]	CH1[13]	CH1[12]	CH1[11]	CH1[10]	CH1[9]	CH1[8]	0x00	R
0x05	Ch2_LSB	CH2[7]	CH2[6]	CH2[5]	CH2[4]	CH2[3]	CH2[2]	CH2[1]	CH2[0]	0x00	R
0x06	Ch2_MSB	CH2[15]	CH2[14]	CH2[13]	CH2[12]	CH2[11]	CH2[10]	CH2[9]	CH2[8]	0x00	R
0x07	Ch3 _LSB	CH3[7]	CH3[6]	CH3[5]	CH3[4]	CH3[3]	CH3[2]	CH3[1]	CH3[0]	0x00	R
0x08	Ch3_MSB	CH3[15]	CH3[14]	CH3[13]	CH3[12]	CH3[11]	CH3[10]	CH3[9]	CH3[8]	0x00	R

Table 13. *Output Register Data Description*

Full Scale Negative Reading	Full Scale Positive Reading	Comments
0x8000	0x7FFF	Sign-extended, 2's complement number. Results in registers: CH1_MSB, CH1_LSB, CH2 _MSB, CH2_LSB, CH3_MSB, CH3_LSB
(-32,768)	(+32,767)	(Typical integer interpretation)

6.4 [0x0A] STATE - Magnetic Sensor State

This register is used to configure the magnetic sensor state.

Table 14. *State Register*

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0A	STATE	0	0	0	0	0	STATE [2]	STATE [1]	STATE [0]	0x00	R/W

The state bit settings are shown in the table below.

Table 15. *State Bit Settings*

STATE[2:0]	State
000	Standby
001	Measurement

6.5 [0x0B] Range - Magnetic Field Range

These registers are used to define the magnetic field range.

Table 16. *Filed Range Register*

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0B	RANGE	RNGE _21[3]	RNGE _21 [2]	RNGE _21 [1]	RNGE _21 [0]	RNGE _3[3]	RNGE _3[2]	RNGE _3[1]	RNGE _3[0]	0x34	R/W

RNGE_21 is for X/Y axis and RNGE_3 is for Z axis.

The value in this register is the absolute number.

Table 17. *Range Bit Settings*

RNGE_21[3:0]	RNGE_3[3:0]	Field Range(±μT)
0001	0010	2200
0011	0100	1200

6.6 [0x11] SWR - Software Reset

Set the SWR bits to logic 1(0x81) will cause this device to perform software-reset—all registers will be returned to their default values and the state machine will be reset. This bit is self-clearing.

Table 22. *Software Reset Register*

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
11	SWR	SWR	0	0	0	0	0	0	SWR	0x00	R/W

7. Contact Us

Please visit Voltafield website at www.voltafield.com for more product information about Voltafield's magnetic sensors or contact us directly via below information.

Voltafield Technology Corporation

Taiwan HQ

6F-1, No. 1, Taiyuan 1st St., Jhubei City, Hsinchu County 30265, Taiwan

Tel / +886-3-6590888*601

Fax / +886-3-6590899

ShenZhen Office

8B, Building 8, No.28, Xianglin Road, Futian District, Shenzhen, China 518040

Tel/ +86-755-2902-4296

Mobile / +86-153-0277-2787

Shanghai Office

Room 2301, No. 7, Lane 300, Nandan East Road, Xuhui District, Shanghai, China 200030

Mobile / +86-156-1808-1621

Bejing Office

Room 104, No. 203, East Wangjinng Garden, Chaoyang District, Beijing, China 100102

Contact e-Mail

sales@voltafield.com

service@voltafield.com